IN THE CLAIMS:

The status of each claim that has been introduced in the above-referenced application is identified in the ensuing listing of the claims. This listing of the claims replaces all previously submitted claims listings.

1-16 (Canceled)

17. (Previously presented) A method of fabricating a fuse upon a semiconductor device, comprising:

disposing a layer of conductive material over an insulative structure of the semiconductor device;

patterning said layer of conductive material to define at least two ~~laterally discrete,~~ spaced apart regions of conductive material ~~between and around which said insulative structure is exposed~~;

disposing a layer of metal silicide over the semiconductor device, including adjacent to ~~said at least two regions and to~~ said insulative structure exposed between ~~and around~~ said at least two regions; and

patterning said layer of metal silicide so as to define at least two terminal regions of the fuse, each of which is in contact with a corresponding one of said at least two regions of conductive material, and a central region disposed between said at least two terminal regions and in contact with said insulative structure.

18. (Original) The method of claim 17, wherein said disposing said layer of conductive material comprises disposing polysilicon onto said insulative structure.

19. (Original) The method of claim 17, wherein said patterning said layer of conductive material comprises disposing a mask over the semiconductor device and removing selected regions of said layer of conductive material through said mask.

20. (Original) The method of claim 19, wherein said disposing said mask comprises:
disposing photoresist onto the semiconductor device;
exposing selected regions of said photoresist; and
developing said selected regions.

21. (Previously presented) The method of claim 19, wherein said removing comprises etching said selected regions of said layer of conductive material through said mask.

22. (Original) The method of claim 21, wherein said etching comprises isotropically etching said selected regions.

E'

23. (Original) The method of claim 21, wherein said etching comprises wet etching said selected regions of said layer of conductive material.

24. (Original) The method of claim 17, wherein said disposing said layer of conductive material comprises chemical vapor depositing said layer of conductive material.

25. (Original) The method of claim 17, wherein said depositing said layer of metal silicide comprises chemical vapor depositing said layer of metal silicide.

26. (Original) The method of claim 17, wherein said depositing said layer of metal silicide comprises depositing tungsten silicide.

27. (Original) The method of claim 17, wherein said patterning said layer of metal silicide comprises disposing a mask over the semiconductor device and removing selected regions of said layer of metal silicide through said mask.

28. (Original) The method of claim 27, wherein said disposing said mask comprises:
disposing photoresist over the semiconductor device;

exposing selected regions of said photoresist; and
developing said selected regions.

29. (Original) The method of claim 27, wherein said removing comprises etching said selected regions of said layer of metal silicide.

30. (Previously presented) The method of claim 29, wherein said etching comprises anisotropically etching said selected regions of said layer of metal silicide.

31. (Previously presented) The method of claim 29, wherein said etching comprises dry etching said selected regions of said layer of metal silicide.

E1

32. (Original) The method of claim 17, further comprising disposing a contact in communication with at least one of said at least two terminal regions.

33. (Original) The method of claim 32, further comprising disposing another contact in communication with another of said at least two terminal regions.

34-49 (Canceled)

50. (Previously presented) A method of fabricating a fuse, comprising:
fabricating laterally discrete, spaced apart regions comprising polysilicon on an insulative structure of a semiconductor device, said insulative structure being exposed between ~~and around~~ each of said spaced apart regions; and
fabricating a fuse comprising a metal silicide, including a central region disposed adjacent the insulative structure and between said spaced apart regions and at least two terminal regions disposed on opposite ends of the central region and adjacent said spaced apart regions.

51. (Original) The method of claim 50, wherein said fabricating spaced apart regions comprises:

disposing polysilicon onto said insulative structure; and

patterning said polysilicon.

52. (Original) The method of claim 51, wherein said disposing polysilicon comprises chemical vapor depositing polysilicon.

53. (Original) The method of claim 51, further comprising doping said polysilicon.

54. (Previously presented) The method of claim 53, wherein said doping occurs substantially simultaneously with said disposing.

E1

55. (Original) The method of claim 51, wherein said patterning comprises disposing a mask adjacent said polysilicon and removing selected regions of said polysilicon through said mask.

56. (Original) The method of claim 55, wherein said disposing said mask comprises disposing photoresist adjacent said polysilicon, exposing selected regions of said photoresist, and developing said selected regions.

57. (Original) The method of claim 55, wherein said removing selected regions of said polysilicon comprises etching said selected regions.

58. (Original) The method of claim 57, wherein said etching comprises isotropically etching said selected regions.

59. (Original) The method of claim 57, wherein said etching comprises wet etching said selected regions.

60. (Previously presented) The method of claim 50, wherein said fabricating said fuse comprises disposing metal silicide adjacent said spaced apart regions and said insulative structure exposed therebetween.

61. (Original) The method of claim 60, wherein said disposing metal silicide comprises chemical vapor depositing metal silicide.

62. (Original) The method of claim 60, wherein said fabricating said fuse further comprises patterning said metal silicide.

63. (Original) The method of claim 62, wherein said patterning comprises disposing a mask adjacent said metal silicide and removing selected regions of said metal silicide through said mask.

64. (Original) The method of claim 63, wherein said disposing said mask comprises disposing photoresist adjacent said metal silicide, exposing selected regions of said photoresist, and developing said selected regions.

65. (Previously presented) The method of claim 63, wherein said removing selected regions of said metal silicide comprises etching said selected regions of said metal silicide.

66. (Original) The method of claim 65, wherein said etching comprises anisotropically etching said selected regions.

67. (Original) The method of claim 65, wherein said etching comprises dry etching said selected regions.

68. (Previously presented) The method of claim 62, wherein said patterning comprises defining said at least two terminal regions of the fuse adjacent said spaced apart regions and said central region of the fuse adjacent said insulative structure.

69. (Original) The method of claim 50, further comprising doping said spaced apart regions of polysilicon.

70. (Original) The method of claim 69, wherein said doping occurs substantially simultaneously with disposing polysilicon on said insulative structure.

71. (Previously presented) A method of substantially simultaneously fabricating a gate and a fuse on a semiconductor substrate, comprising:

disposing a layer of insulative material over at least an exposed region of the semiconductor substrate;

disposing a layer of polysilicon over the semiconductor substrate, including over said layer of insulative material and over field oxide regions disposed on the semiconductor substrate;

patterning at least regions of said layer of polysilicon disposed over at least one field oxide region of said field oxide regions to define at least two laterally discrete, spaced apart regions from said polysilicon over said at least one field oxide region with ~~portions~~ at least a portion of said at least one field oxide region being exposed laterally ~~around each of~~ between said spaced apart regions ~~and therebetween~~;

disposing a layer of metal silicide on said layer of polysilicon and into contact with said ~~portions~~ portion of said at least one field oxide region;

patterning at least said layer of metal silicide to define the fuse and the gate therefrom.

72. (Original) The method of claim 71, wherein said disposing said layer of polysilicon comprises chemical vapor depositing said layer of polysilicon.

73 (Canceled)

74. (Previously presented) The method of claim 71, wherein said defining the fuse comprises defining a central region disposed adjacent and substantially between said at least two spaced apart regions and defining at least two terminal regions, each terminal region continuous with an end of said central region and disposed adjacent one of said at least two spaced apart regions.

75. (Previously presented) The method of claim 71, wherein said defining said at least two spaced apart regions comprises disposing a mask over said layer of polysilicon and removing selected regions of said layer of polysilicon through said mask.

E!

76. (Original) The method of claim 75, wherein said disposing said mask comprises disposing photoresist over said layer of polysilicon, exposing selected regions of said photoresist, and developing said selected regions.

77. (Original) The method of claim 75, wherein said removing comprises etching said layer of polysilicon.

78. (Original) The method of claim 77, wherein said etching comprises wet etching said layer of polysilicon.

79. (Original) The method of claim 77, wherein said etching comprises isotropically etching said layer of polysilicon.

80. (Original) The method of claim 71, further comprising patterning gate regions of said layer of polysilicon.

81. (Original) The method of claim 80, wherein said patterning said gate regions occurs substantially simultaneously with said patterning said at least regions of said layer of polysilicon.

82. (Original) The method of claim 80, wherein said patterning said gate regions comprises disposing a mask over said layer of polysilicon and removing selected regions of said layer of polysilicon through said mask.

83. (Previously presented) The method of claim 82, wherein said disposing said mask comprises disposing photoresist over said layer of polysilicon, exposing selected regions of said photoresist, and developing said selected regions.

E1

84. (Original) The method of claim 82, wherein said removing comprises etching said selected regions.

85. (Original) The method of claim 84, wherein said etching comprises dry etching said selected regions.

86. (Original) The method of claim 84, wherein said etching comprises anisotropically etching said selected regions.

87. (Original) The method of claim 71, wherein said disposing said layer of metal silicide comprises chemical vapor depositing said layer of metal silicide.

88. (Original) The method of claim 71, wherein said defining the fuse and the gate from at least said layer of metal silicide comprises disposing a mask over said layer of metal silicide and removing selected regions of said layer of metal silicide through said mask.

89. (Previously presented) The method of claim 88, wherein said disposing said mask comprises disposing photoresist over said layer of metal silicide, exposing selected regions of said photoresist, and developing said selected regions.

90. (Original) The method of claim 88, wherein said removing said selected regions comprises etching said selected regions.

91. (Original) The method of claim 90, wherein said etching comprises dry etching said selected regions.

92. (Original) The method of claim 90, wherein said etching comprises anisotropically etching said selected regions.

E1

93. (Original) The method of claim 71, further comprising removing exposed regions of polysilicon through said layer of metal silicide.

94. (Original) The method of claim 93, wherein said removing comprises etching said exposed regions.

95. (Original) The method of claim 94, wherein said etching comprises dry etching said exposed regions.

96. (Original) The method of claim 94, wherein said etching comprises anisotropically etching said exposed regions.

97. (Original) The method of claim 93, further comprising removing exposed regions of said layer of insulative material through said layer of polysilicon.

98. (Previously presented) The method of claim 97, wherein said removing said exposed regions of said layer of insulative material comprises etching said exposed regions of said layer of insulative material.

99. (Previously presented) The method of claim 98, wherein said etching comprises dry etching said exposed regions of said layer of insulative material.

100. (Previously presented) The method of claim 98, wherein said etching comprises anisotropically etching said exposed regions of said layer of insulative material.

101. (Previously presented) The method of claim 71, further comprising doping at least one source region and at least one drain region of the semiconductor substrate, said at least one source region and said at least one drain region disposable adjacent the gate on opposite sides thereof.